2.0 BLOCK DIAGRAM

Figure 2-1 shows the functional components of the power amplifier module.

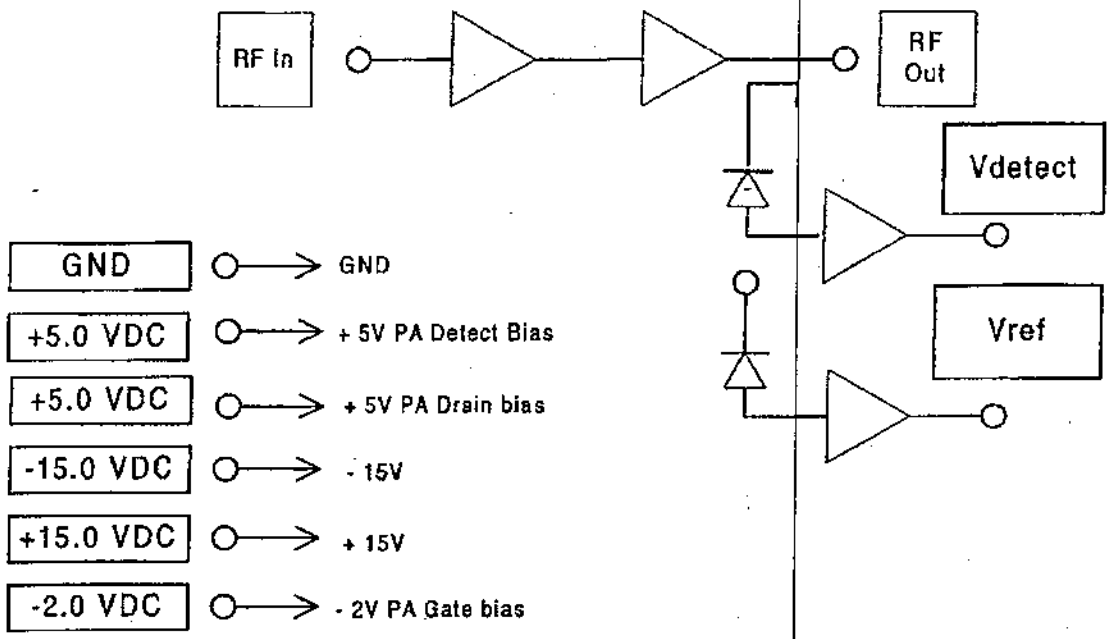

Figure 2-1 Power Amplifier Block Diagram

3.0 ELECTRICAL SPECIFICATION

See **Figure 2-1** for Power Amplifier Block Diagram.

Electrical specifications apply over operating temperature range unless otherwise noted.
All specifications are for –0001 and –0002 unless otherwise noted.

Operating frequency band:	
-0001	38.6-40GHz
-0002	24.25-25.25GHz
Output Power @ 1dB compression point:	27dBm
Transmit Adjacent Channel Power:	
-0001	36 dBc minimum at Pout ≤ 17.3 dBm
-0002	37 dBc minimum at Pout ≤ 16.0 dBm
	10 Ms/s sq. Root Raised Cosine ∝=0.21 64 QAM for both –0001 and –0002
Input Return Loss:	10 dB minimum
Output Return Loss:	10 dB minimum
Gain:	35.0 dB nominal
Gain variation over temp. and freq.:	± 5.0 dB
Gain flatness:	± 0.05 dB over any 12.5 MHz channel
Linear gain expansion**:	1 dB maximum (from P_{1dB} –20dB to P_{1dB})
Output Noise Density:	-124 dBm/Hz
Maximum input power level:	+13 dBm
Stability:	No oscillation when either port is terminated in an open or short circuit at any phase.
V_{detect} @ 25 dBm:	- 1.6 ± 0.5 V***
V_{detect} @ 10 dBm:	+ 0.3 ± 0.4 V ***
V_{detect} (no power):	+ 0.5V ± 0.3 V***
V_{ref} (no power):	+ 0.5V ± 0.3 V*** (shall remain constant over entire RF range)
$V_{ref} - V_{detect}$ (no power):	0.00V ± 0.05V***
Detector output characteristics:	Shall be monotonic and have a minimum slope of 20mv/dB over the RF power range of 10 to 25 dBm. Shall also be monotonic at RF power levels which are less than 10dBm (i.e. output shall be greater than the voltage at 10 dBm for power levels less than 10 dBm).
Detector 3dB corner frequency:	800 kHz ± 20%
Mute from P_{1dB} compression to off:	80 dB minimum

** gain expansion measured relative to the linear operating point (i.e., gain relative to 20 dB backoff from P_{1dB}).

*** measured with RF load VSWR of 1.2 maximum, and DC load of 7 k ohm minimum.

3.1 POWER SUPPLY

Supply voltage:

+5V PA Drain Bias:	+5.0 VDC ±2% at 2.2A maximum
-2V PA Gate Bias:	-2.0 VDC ±2% at 25 mA maximum
+15V:	+15.0 VDC ±5% at 25 mA maximum
-15V:	-15.0 VDC ±5% at 25 mA maximum
+5V PA Detect Bias	+5.0 VDC ±2% at 10 mA maximum
Power Supply rejection:	Gate bias filtering (-2V line) must be provided to reject interfering frequencies in the range of 200 kHz to 2GHz; rejection level 20 dB

Table 3-1 Absolute Maximum Voltage Ratings (continuous unless noted otherwise)

No.	Item	Limit	
		Minimum	Maximum
1	+5V PA Drain Bias	-0.6V	+5.25V
		-0.6V	+5.50V (<10 seconds)
2	-2V PA Gate Bias	-4V	+0.6V
3	+15V	-0.6V	+24V
4	-15V	+0.6V	-24V
5	+5V PA Detect Bias	-0.6V	+6V

4.0 EXTERNAL INTERFACES

Table 4-1shows the connector names and description.

Table 4-1 Connector Description

Connector	Model Type		Signal Description
J1	14 Pin 0.1 x 0.1 Header Berg P/N: 88880-037 or equivalent		See **Table 4-2** for description.
J2	-0001 WR-28	See outline drawing in **Section 5.0** *	RF Input
	-0002 WR-34		
J3	-0001 WR-28	See outline drawing in **Section 5.0** *	RF Output
	-0002 WR-34		

* Note: Waveguide dimensions per EIA RS 261 Rect. Waveguide.

Table 4-2 J1 Connector Pin Layout

Reference Designator	Signal Description
J1 – Pin 1	+5V PA Drain Bias
J1 – Pin 2	+5V PA Drain Bias
J1 – Pin 3	GND
J1 – Pin 4	GND
J1 – Pin 5	Vdetect
J1 – Pin 6	-15V
J1 – Pin 7	+5V PA Drain Bias
J1 – Pin 8	+5V PA Drain Bias
J1 – Pin 9	Vref
J1 – Pin 10	+5V PA Detect Bias
J1 – Pin 11	+15V
J1 – Pin 12	GND
J1 – Pin 13	-2V PA Gate Bias
J1 – Pin 14	GND

5.0 MECHANICAL SPECIFICATIONS

5.1 MECHANICAL OUTLINE

NOTES (UNLESS OTHERWISE SPECIFIED):

1. Dimensioning and Tolerancing Per ANSI Y14.5M-1994.
2. No burrs Or Loose Particles Allowed.
3. Surface Indicated Used For Mounting/Interface.
4. K eep Out Area.

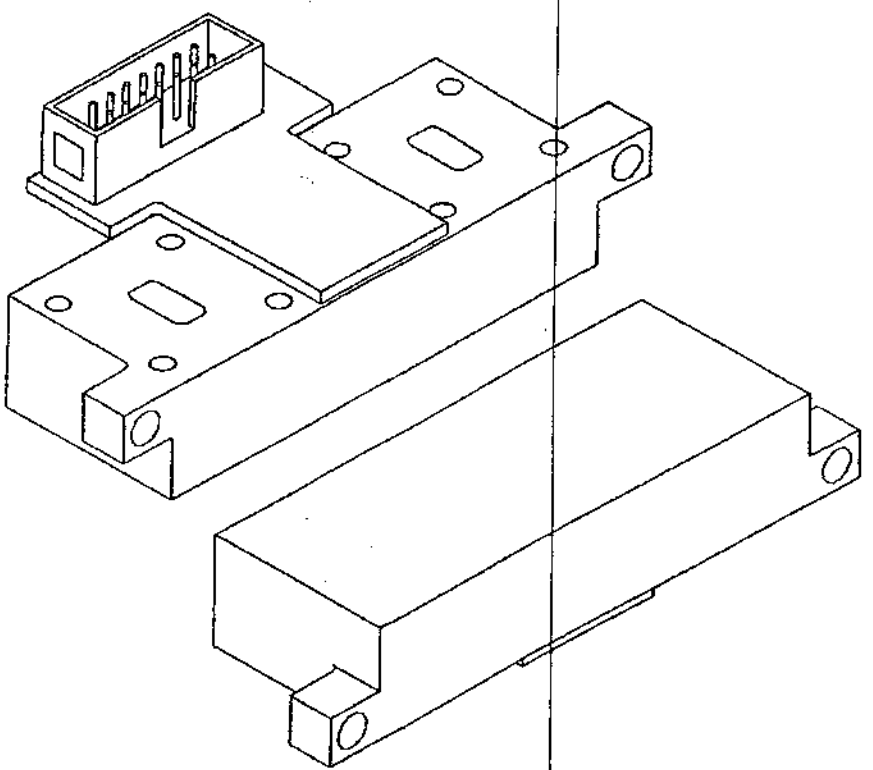

Figure 5-1 PA Overview

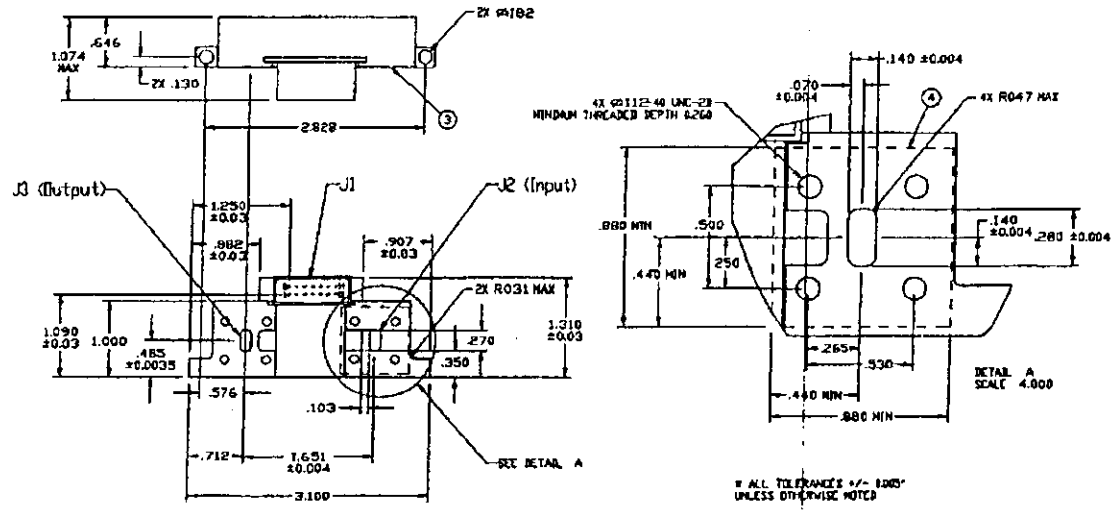

Figure 5-2 38 GHz Package A

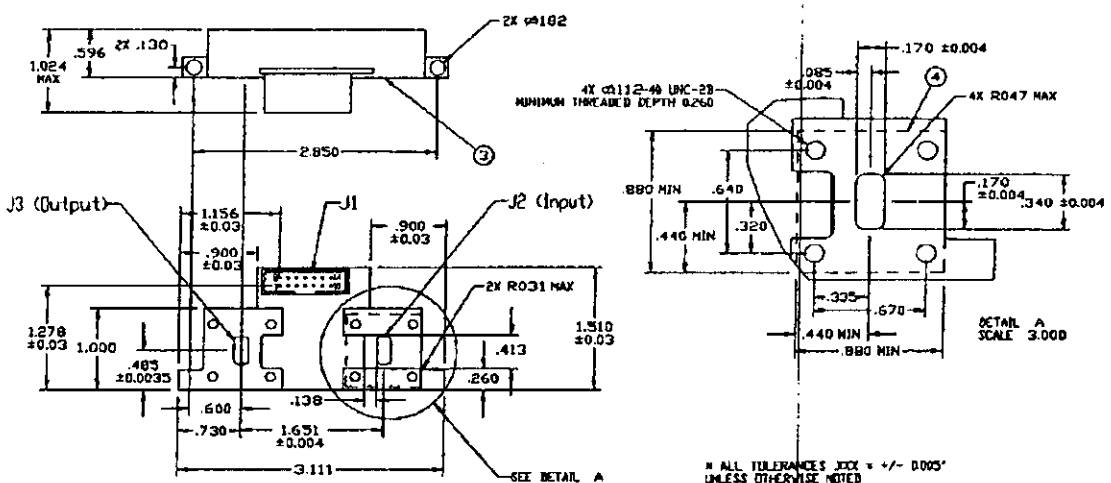

Figure 5-3 24 GHz Package B